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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,775	02/06/2002	Igor Anatolievich Abrosimov	033533-001	5820

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EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,775	ABROSIMOV ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *080802*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 15 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 15 and 19: "for example" makes the preceding limitation indefinite.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,138,259 to Tsuto *et al* (hereafter "Tsuto") in view of U.S. Patent No. 4,965,799 to Green *et al* (hereafter "Green").

Fig. 4 of Tsuto shows a DRAM chip testing system including a data-transmitting "data transferring apparatus having a data input and a data output" (12), a "plurality of data transferring sections operable in parallel for transferring data" (21A, 21B), and clock generator logic (14, 15) generating a "full-frequency" clock signal and a "low-frequency" clock signal, with "the low frequency being a quotient of the full frequency and the number of data transferring operations". The "low-frequency" clock signal is

output from a clock/select signal generator unit (15) and has a frequency of 1/N, where N=2 is the number of "data transferring sections". Tsuto's Fig. 4 also shows a "circuit for synchronizing said parallel data transferring sections" (100).

Regarding claims 1, 7 and 10, Tsuto does not describe the clock frequencies as being "programmable". Green discloses providing a memory chip testing system with a variable (i.e. programmable) frequency test clock in order to advantageously determine the maximum operating frequency of the memory chip. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Tsuto's clock generator with a programmable frequency. Such a realization would have been obvious because Green teaches that a variable (i.e. programmable) frequency test clock permits the maximum operating frequency of the memory chip to be advantageously determined.

Regarding claims 2-4, 9, 11, 12 and 17, Tsuto's Fig. 4 also shows a high-speed converter unit (16) serving as a "multiplexer for receiving data from said data transferring sections at said low frequency and providing output data at said high frequency", and can also be described as a "resynchronization circuit for resynchronizing data received at low frequency to a system clock signal of full frequency".

Regarding claims 5, 6 and 14, Tsuto's comparison logic (13A, 13B) also serves as a "plurality of data transferring sections" that are "data receivers".

Regarding claims 8, 16 and 20, although Tsuto teaches that "N" referred to above can be a value other than N=2, however Tsuto does not specifically mention

N=4. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Tsuto's testing system wherein the above-mentioned value of "N" is four. Such an implementation would have been obvious because Tsuto teaches that "N" referred to above can be a value other than N=2.

Regarding claims 13 and 18, Tsuto's logic comparators (13A, 13B) generate fault data from the memory testing, and thus also serve as "fault logic devices".

Further regarding claim 18, Tsuto does not specifically mention latching input and output data of Tsuto's low speed converter unit (17). Official Notice is given that the data stabilizing and retaining advantages provided by data latching were well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Tsuto's low-speed converter unit with data latching at the inputs and outputs. Such an implementation would have been obvious because the data stabilizing and retaining advantages provided by data latching were already well known.

Regarding claims 15 and 19, and further regarding claims 16 and 20, although Tsuto's tester is disclosed to be for testing of DRAMs, Tsuto does not specifically mention using the memory testing system for testing of SDRAMs or DDR SDRAMs. Official Notice is taken that SDRAMs and DDR SDRAMs were well-known types of DRAM at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply Tsuto's DRAM testing system to the testing of SDRAMs and DDR SDRAMs. Such an

application would have been obvious because SDRAMs and DDR SDRAMs were already well-known types of DRAM.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133